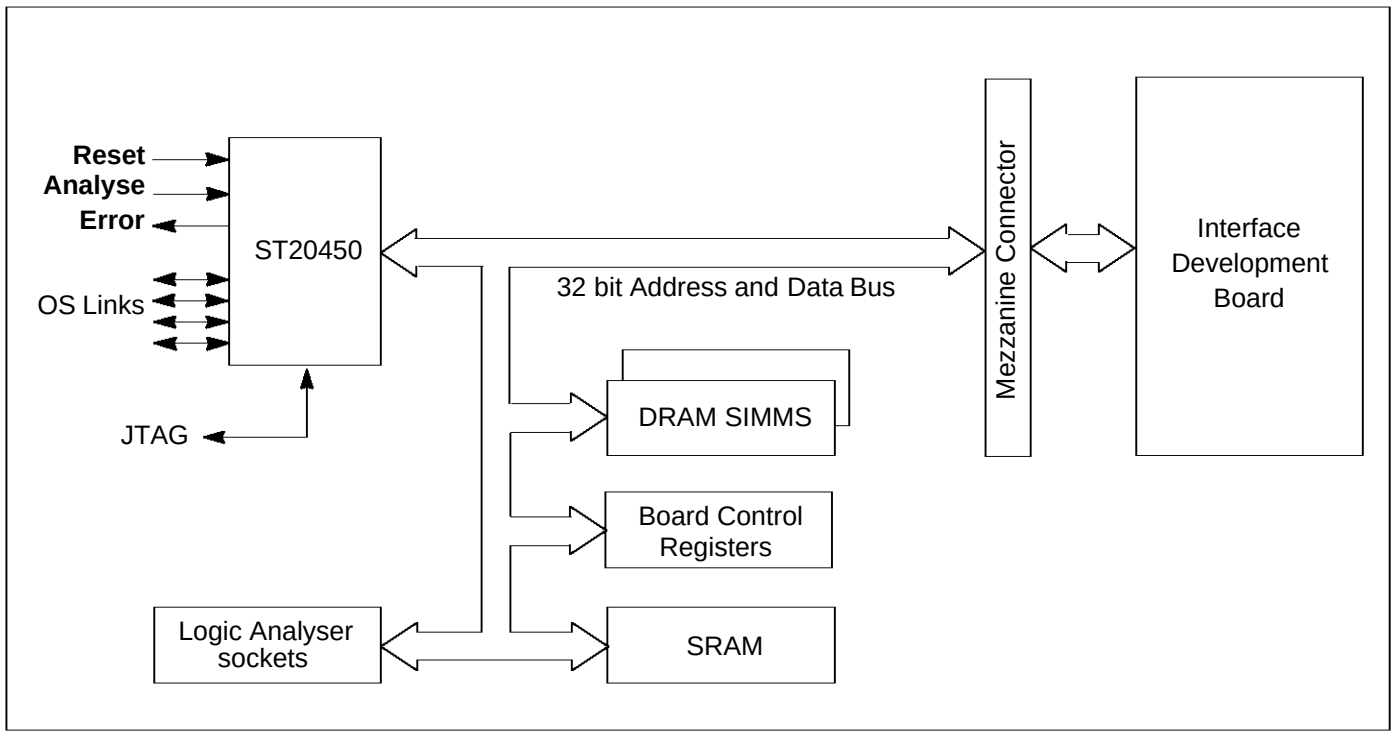
SGS-THOMSON MICROELECTRONICS

ST20450 Development Board

VME FORMAT MULTI-ROLE PLATFORM

PRODUCT INFORMATION



FEATURES

- Flexible evaluation platform for the ST20450 32 bit processor
- VME rack or benchtop use
- Fast SRAM memory system for benchmarking algorithms
- Use upgradeable DRAM to support programs up to 64MByte
- Prototyping of peripheral interfaces via mezzanine I/O card connector
- Single 5V power rail. 3.3V derived on board
- Front and back panel access to development sytem connection

DESCRIPTION

The ST20450 Development Board is a development and interface prototyping platform for the ST20450 processor - the first in the family of processors based on the SGS-THOMSON ST20 Microprocessor Core.

A variety of memory system options are provided as standard in conjunction with a socket for a user designed mezzanine I/O board. An ST20 host/target development connection is supported in both differential and single ended form. The board can be mounted in a standard VME rack or used on the bench top. A set of on-board connectors allows quick and convenient interfacing to the HP 16500 series of Logic Analyser Systems for hardware performance analysis and debugging.

Contents

1 Introduction

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2 Hardware overview

The overall block diagram of the ST20450 Development Board is shown in Figure 2.1. The type and organisation of the external interfaces is intended to offer a flexible range of options for an application developer, both in terms of performance modelling and data/code residency. Connections to the development host are standardised, as are the pod assignments for the HP16500 logic analyser tools. A range of configuration and performance options are selected by well labelled jumper connectors.

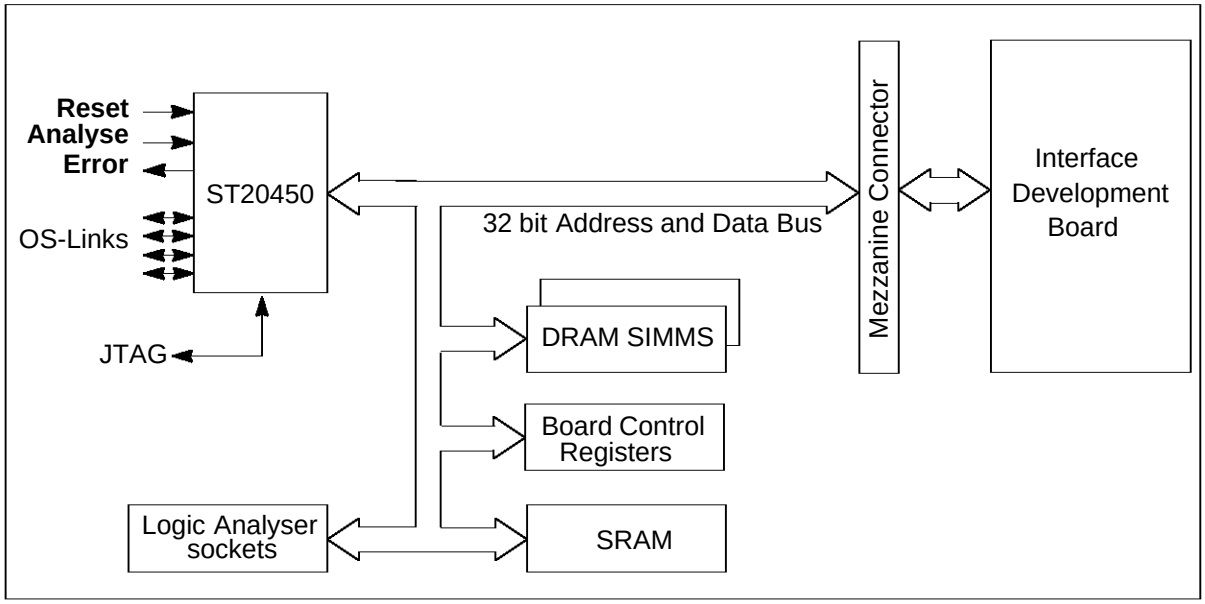

Figure 2.1 Block diagram

The principle features of the board are:

- VME format board allowing in-rack or desktop usage
- 512Kbytes of fast 2 cycle SRAM for optimum benchmarking performance. Using jumpers the bus width of this memory block can be selected as 8, 16 or 32 bits. Using the programmable ST20450 EMI, a range of cycle times can be modelled to understand the performance issues in a given system design.
- Standard 72 pin 5V SIMM sockets for user DRAM installation of up to 64Mbytes. SIMM type can be sensed by the processor before memory configuration
- 128 pin connector for interface to a user defined mezzanine I/O board. The connector pinout includes power, interrupt and DMA control signals.
- Pod sockets for standardised connection to HP16500 series Logic Analyser Systems. These LAS products can be used to analyse real-time I/O and memory traffic along with peripheral activity. Standard setup files, including a disassembler module is available for the ST20 instruction set.
- Single 5V power rail required. An on-board 3.3V dc-dc connector module provides dual power supplies for circuit components.
- Standard single ended OS-Link subsystem connection via P2 and differential to front panel.
- VME OS-Link P2 link/**Reset**, **Analyse** and **Error** (RAE) pinout compatible with IMS B014 P2 pinout.
- Jumper block for Boot options (Boot source, Link speed, processor speed, disable internal SRAM)
- Board configuration/status registers for DRAM SIMM size and speed status, **Reset**, **Analyse** and **Error** (RAE) subsystem down.

3 Installation

3.1 Anti-static precautions

The ST20450 Development Board contains MOS devices and in common with all boards of this type some handling precautions need to be observed.

Only handle the board by its edges or the front panel and avoid touching the rear connector pins.

To ensure that no damage occurs to the MOS devices on the board, static discharges onto the board must be avoided. The board is shipped in an anti-static bag which provides protection during shipping and should not be opened until the board is going to be installed.

Static discharges will only occur between objects that are at a different electrical potential. A good procedure to employ is to ensure that yourself, the board to be

installed and any rack to be used, are at the same electrical potential. This can be achieved by touching an exposed metal surface of the rack casing while at the same time holding the anti-static bag containing the ST20450 Development Board.

3.2 VME rack compatibility

The ST20450 Development Board conforms to the physical aspects of the VME card specification.

The P1 connector of the VMEbus is used for only a small subset of its signals, its principle use being to supply power to the board. The pin assignment of the P1 connector is given in Table 11.1.

Via the P2 VME connector a set of OS-Link signals are provided to support close coupling of the ST20450 Development Board interface and hardware within the same physical enclosure. The pin assignment for the P2 connector is given in Table 11.2.

3.3 Bench-top usage

When using the board on a bench-top, it must be placed on a non-conductive surface, or fitted with rubber feet to prevent electrical and physical damage, (refer to section 3.4 also). A flying lead terminated with a disk drive type connector should be used to connect a 5V benchtop PSU.

3.4 ESD protection

If the ST20450 Development Board is not rack mounted and is used in a stand-alone manner on the bench-top, it must be located in a static free environment. Therefore it must be placed on a grounded anti-static mat and the necessary anti-static precautions maintained at all times. For example, the user must always wear a wrist strap (connected to the mat) for grounding purposes.

4 Physical layout and jumpers

The physical layout of the ST20450 Development Board (viewed from above) is shown in Figure 4.1.

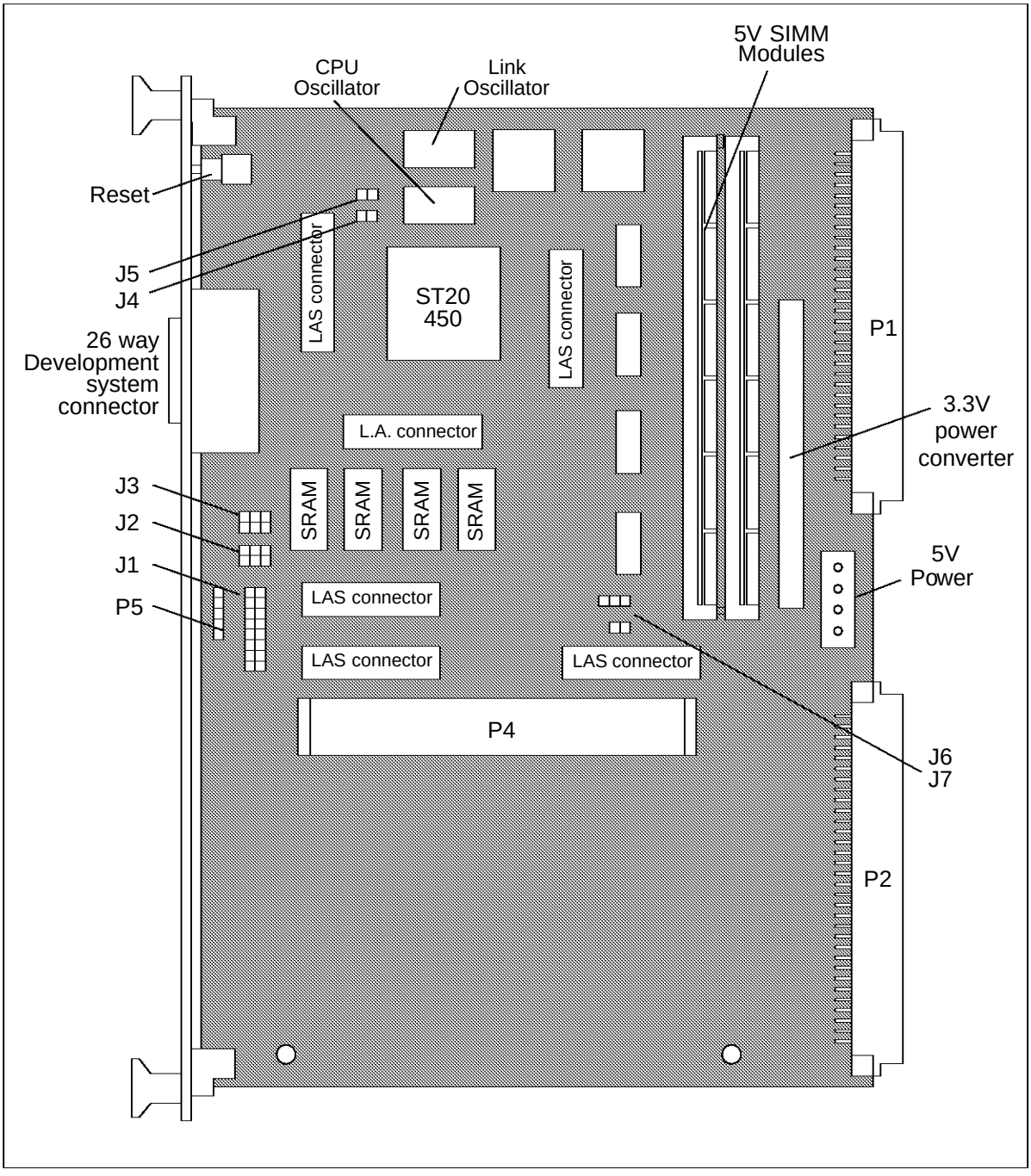

Figure 4.1 Board layout

5 Memory I/O system

The overall memory map of the ST20450 Development Board is shown in Figure 5.1. The details of the contents of each bank are discussed in subsequent sections.

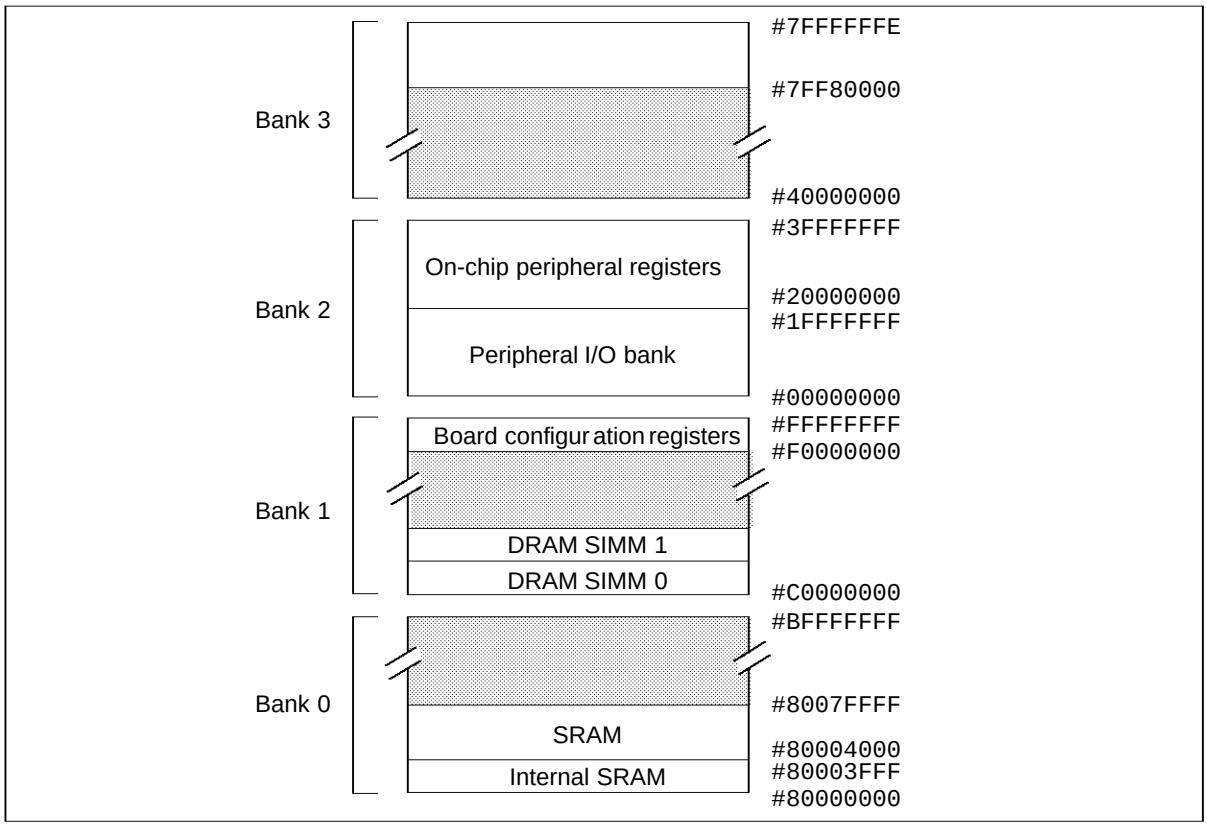

Figure 5.1 ST20450 Development Board memory map

5.1 Register definitions

Register	R/W	Hexadecimal Address	Valid Bit(s)
VppGen	R/W	F0000000	0
ResetDown	R/W	F0800000	0
AnalyseDown	R/W	F1000000	0
ErrorDown	R	F1800000	0
IntTimerValueReg	W	F4000000	5:0
InterruptGenDisable	R/W	F4800000	0

Table 5.1 Register definitions

On all reads from these register locations, bits 15:8 correspond to the SIMM PD pins-bit11-bit8 for SIMM PD0 and bit15-bit12 for SIMM PD1. Refer to Table 7.1 and Table 7.2 for expected values from these pins. When no devices are installed the bits will read as ‘1’s.

5.2 Register descriptions

Register	Description
ResetDown **AnalyseDown** **ErrorDown**	These three registers are associated with the P2 and front panel OS **SubSystemDown** port. Both the front panel and P2 pins are active simultaneously and as such a write of 1 to the reset port will enable reset on both the P5 and P2 connectors. When reading **Error** this is an OR of the P2 and P5 connector **Error** pins. Note that the **Reset, Analyse** and **Error** signals on P2 and P5 are active low signals whereas the registers are active high.
Interrupt Generator	The Interrupt Generator consists of two registers. **IntTimerValueReg** contains the period between interrupts, and the **InterruptGenDisable** register is used to enable or disable the generator. The Interrupt Generator is based on a 10 bit programmable countdown counter. The six most significant bits are programmable using the **IntTimerValueReg**, which sets the period between interrupts. The four least significant bits are set to 0. Once enabled, the counter counts down this 10 bit value to 0. A 5MHz oscillator is used to clock the counter and when it reaches 0 the **Interrupt2** is set. On the next clock cycle the counter is set to the **IntTimerValueReg** and the interrupt pin cleared ready for the next interrupt cycle.

Figure 5.2

6 SRAM

The SRAM on the board is made up of four 128Kx8 17ns SRAM. These are connected directly to the ST20450 to provide a 2 cycle memory bank - the fastest possible external memory subsystem.

6.1 Strobe definitions

The ST20450 memory strobes are defined for bank 0 as follows:

- **notMemRAS** not connected in this bank
- **notMemCAS** used as **notCE** of SRAM
- **notMemPS** used as **notOE** of SRAM
- **notMemWrBE(3:0)** used as Byte **notWR**’s of SRAM

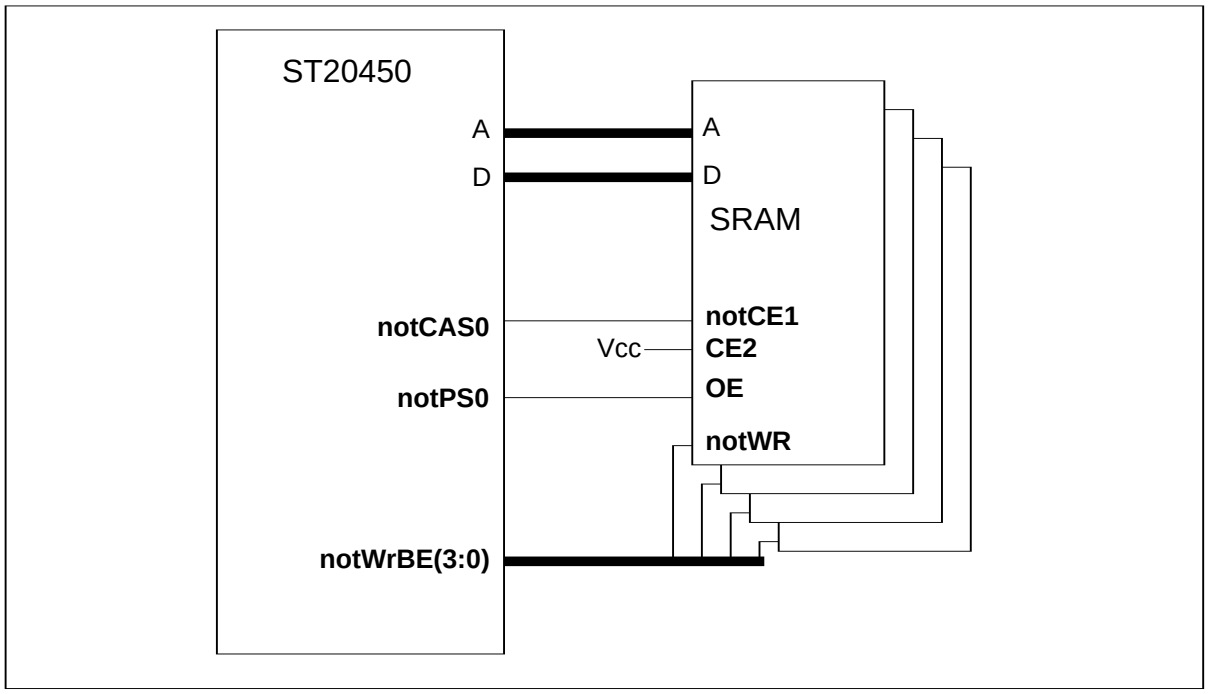

Figure 6.1 SRAM block diagram

6.2 Changing bus widths

The SRAM in bank 0 can be used in 8, 16 or 32 bit mode, allowing the user to evaluate the effectiveness of different cost/performance options. By default, the board comes configured to use a 32 bit bus width and the memory configuration used to program the EMI should reflect this. To change from one bus width to another, both the bus width parameter in the EMI configuration and jumper J2 need to be changed. The positions used for J2 are shown in Figure 6.2.

As the bus width is reduced, so the total amount of SRAM available is also reduced. Thus for 16 bit mode, only 256K is available and only 128K for 8 bit mode.

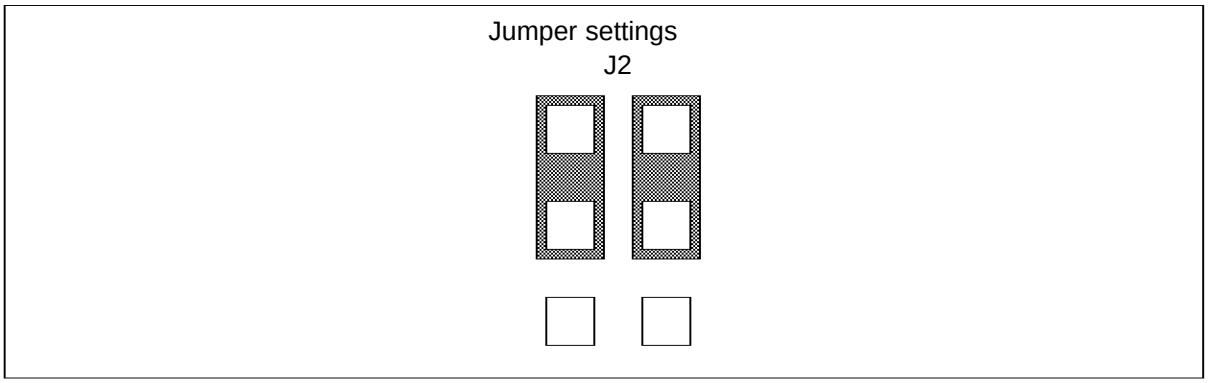

Figure 6.2 SRAM bus width jumper settings - 32 bit mode (default)

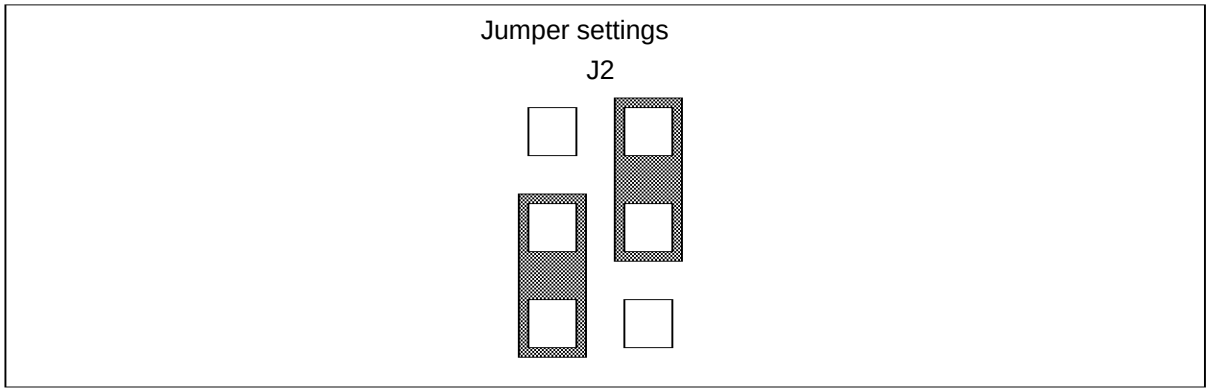

Figure 6.3 SRAM bus width jumper settings -16bit mode

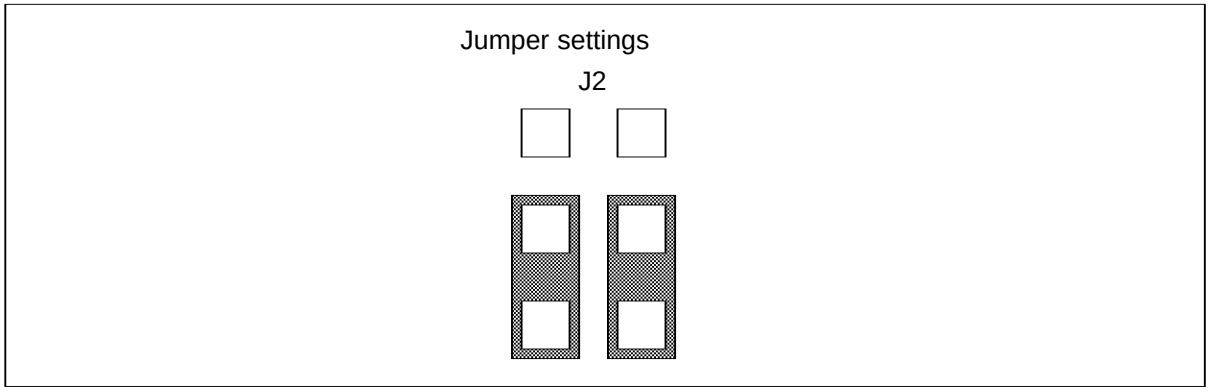

Figure 6.4 SRAM bus width jumper settings - 8 bit mode

7 DRAM and SIMM options

The ST B450 uses an EPLD device to provide SIMM bank decoding within the region of ST20450 memory bank 1 and also allows the mezzanine peripheral interface card DMA access to the DRAM.

7.1 DRAM Decode

The SIMM PD pins denote what speed and size of SIMM is installed. The size code (PD0, PD1) for the smallest SIMMs are the same as those of the larger ones. Therefore the board is configured to assume that larger SIMMs are present, preventing small sized SIMMs from being used on the board. The use of SIMMS smaller than 1MByte by 32 will result in gaps within the DRAM memory map.

Valid SIMM sizes are:

- 1MByte by 32 or 36
- 2MByte by 32 or 36

- 4MByte by 32 or 36
- 8MByte by 32 or 36

Note: No SIMM devices are supplied with the board in its standard configuration.

Figure 7.1 shows the DRAM SIMM interface used.

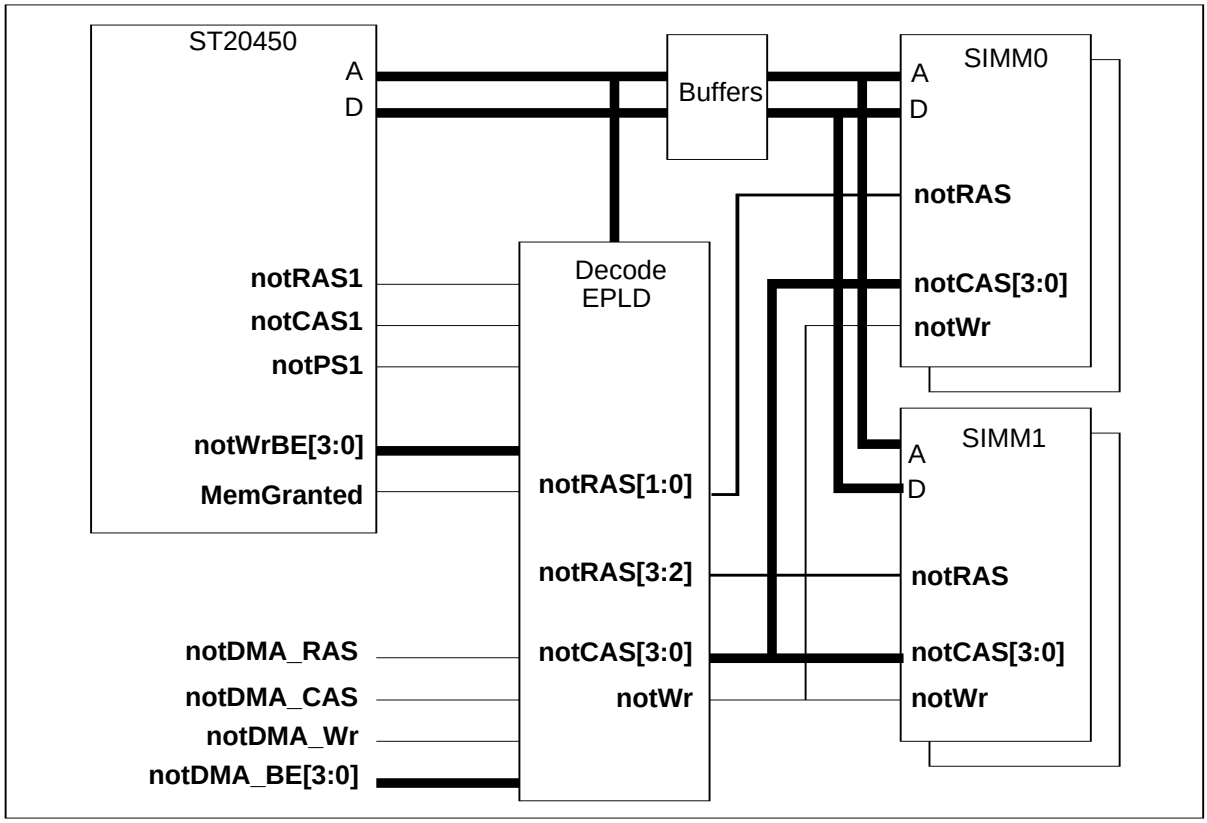

Figure 7.1 DRAM block diagram

SIMM PD codes

The Presence Detect (PD) codes are as follows:

SIMM	PD1	PD0
1M by 36	1	1
2M by 36	0	0
4M by 36	0	1
8M by 36	1	0

Table 7.1 DRAM SIMM PD 0-1 coding

Speed	PD3	PD2
60ns	0	0
70ns	0	1
80ns	1	0

Table 7.2 DRAM SIMM PD 2-3 coding

These SIMM PD codes can be read in the software using a 'word read' from any of the board registers such as the **VppGen** register.

Bits 11:8 are PD3:0 of SIMM0

Bits 15:12 are PD3:0 of SIMM1

The board uses PD0 and PD1 of SIMM0 to detect which type of address mapping to use in its bank decode. Both SIMMs must be the same size since only PD1:0 on SIMM0 is used. DRAM contiguity cannot be guaranteed if different sized SIMMs are used. Different speeds can be used, but the software will need to be designed to detect which SIMM is the slowest and program the EMI for that speed.

One SIMM can be fitted, but should be present in the SIMM 0 socket.

If automatic memory configuration is required, the software should boot-up initially in a slow 4Mbyte configuration, read the SIMM PD bits and reconfigure accordingly. The bank must be configured initially before being able to read from any of the board registers.

8 Reset circuitry

The board has several sources of reset:

- Front panel push button
- Power on reset
- VME **SysReset**
- Front panel OS subsystem
- P2 RAE subsystem

Both the front panel reset push button, **SysReset** and power on reset will toggle the **notRST** pin of the ST20450. The OS subsystem reset pins toggle the **CPUreset** pin only. The mezzanine connector reset is connected to the **CPUreset**.

9 Option jumpers (J1)

The J1 jumpers are used to configure various options for the ST20450. If a shorting link is present on the jumper, the pin is at logic 0 and if it is absent, the pin is at logic 1. gives a description of each jumper. Further descriptions of the pins can be found in [1]

Jumper	Function	Comment
J1-1	Disables internal RAM	0 = Use internal RAM (Default) 1= Disable internal RAM
J1-2/3	Boot source	Sets boot from link on ROM and ROM bus width. 00 = Boot from link (Default) 10 = 16 bit ROM 11 = 8 bit ROM
J1-4	**LinkSpecial**	Refer to Table 9.2
J1-5	**LinkSpeed0**	Refer to Table 9.2
J1-6	**LinkSpeed1**	Refer to Table 9.2
J1-7	**ProcSpeed0**	Refer to Table 9.3
J1-8	**ProcSpeed1**	Refer to Table 9.3
J1-9	**ProcSpeed2**	Refer to Table 9.3

Table 9.1 Option jumper

LinkSpeed1	LinkSpeed0	Link0Special	Link1-3 speed	Link0 speed
0	0	X	TimesOneMode	TimesOneMode
0	1	0	10 Mbits/s	10 Mbits/s
1	0	0	20 Mbits/s	20 Mbits/s
1	1	X	RESERVED	RESERVED
0	1	1	10 Mbits/s	5 Mbits/s
1	0	1	20 Mbits/s	10 Mbits/s

Table 9.2 Link speed settings

ProcSpeed2	ProcSpeed1	ProcSpeed0	Processor clock speed MHz	Processor cycle time ns	Phase lock loop factor (PLLx)	Allowable ClockIn range MHz
0	0	0	TimesOneMode			0 - 32
0	0	1	RESERVED			RESERVED
0	1	0	RESERVED			RESERVED
0	1	1	30	33.3	6	5 - 8.3
1	0	0	40	25.0	8	4 - 6.25
1	0	1	RESERVED			RESERVED
1	1	0	RESERVED			RESERVED
1	1	1	RESERVED			RESERVED

Table 9.3 Processor speed selection

10 External power

The 5V power to the ST20450 Development Board can be supplied by installing the board in a standard VME rack or by powering from a flying lead to an onboard disk drive type connector. The pinout for this power connector is given in Figure 10.1.

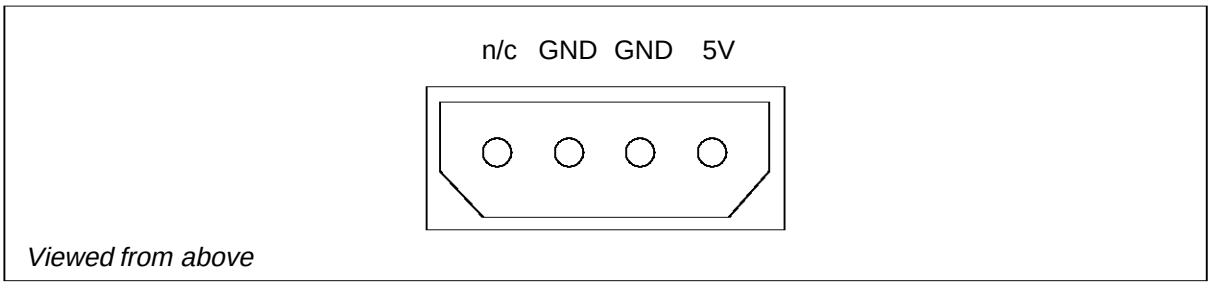

Figure 10.1

11 Development system connections

The board has two options for the connection to a development host via an OS-Link:

- Front panel differential connector
- Single ended links and control signals on the VME P2 connector.

OS-Link 0 of the ST20450 is jumper selectable via J3 to come from either the front panel 26-way high-density connector or via the VME P2 connector.

Both the front panel and P2 control subsystems can reset the board. The **ErrorOut** signal of the ST20450 is fed to both subsystems.

11.1 P1 and P2

The P1 connector supports a standard set of VMEbus compatible pins including power and **SysReset.** The ST20450 Development Board does not participate in any VMEbus transactions, but can co-exist in a rack with standard CPU and peripheral cards.

The P2 connector supports all four OS-Links from the ST20450 including both subsystem up and subsystem down **Reset, Analyse** and **Error** (**RAE**) signals.

Note: SubsystemDown (as far as the control registers for the ST20450 are concerned) is not a standard subsystem as its address location enables Bank 2 to be kept free for mezzanine peripherals. Refer to Table 11.2 or the P2 connector pinout.

Pin	Row C	Row B	Row A
1			
2			
3			
4		***BG0IN**	
5		***BG0OUT**	
6		***BG1IN**	
7		***BG1OUT**	
8		***BG2IN**	
9	**GND**	***BG2OUT**	**GND**
10		***BG3IN**	
11		***BG3OUT**	**GND**
12	***SYSRESET**		
13			
14			
15			**GND**
16			
17			**GND**
18			
19			**GND**
20		**GND**	
21			*** IACKIN**
22			***IACKOUT**
23		**GND**	
24			
25			
26			
27			
28			
29			
30			
31	**+12V**		
32	**+5V**	**+5V**	**+5V**

Note: All remaining pins are not connected

Table 11.1 STB40 P1 connector pinout

Pin	Row C	Row B	Row A
1	**GND**	**VCC**	
2	**nc**	**GND**	
3	**Link0Out**		
4	**Link0In**		
5	**GND**		
6	**GND**		
7	**nc**		
8	**Link1Out**		
9	**Link1In**		
10	**GND**		
11	**GND**		
12	**nc**	**GND**	
13	**Link2Out**	**VCC**	
14	**Link2In**		
15	**GND**		
16	**GND**		
17	**nc**		
18	**Link3Out**		
19	**Link3In**		
20	**GND**		
21			
22		**GND**	
23			
24			
25			
26			
27			
28	**notBackUpReset**		**notBackDownReset**
29	**notBackUpAnalyse**		**notBackDownAnalyse**
30	**notBackUpError**		**notBackDownError**
31	**GND**	**GND**	**GND**
32	**GND**	**VCC**	**GND**

Table 11.2 ST20450 Development Board P2 connector pinout

11.2 Front Panel

The front panel differential development system connector is pin compatible with the IMS B019, IMS B300 and IMS B103 products. Cables supporting this connection are also available.

Caution: When using the IMS CA15 differential cable to connect to an IMS B300, care must be taken to ensure that it is not connected to **Link0** of the IMS B300 as this will result in reset latch-up.

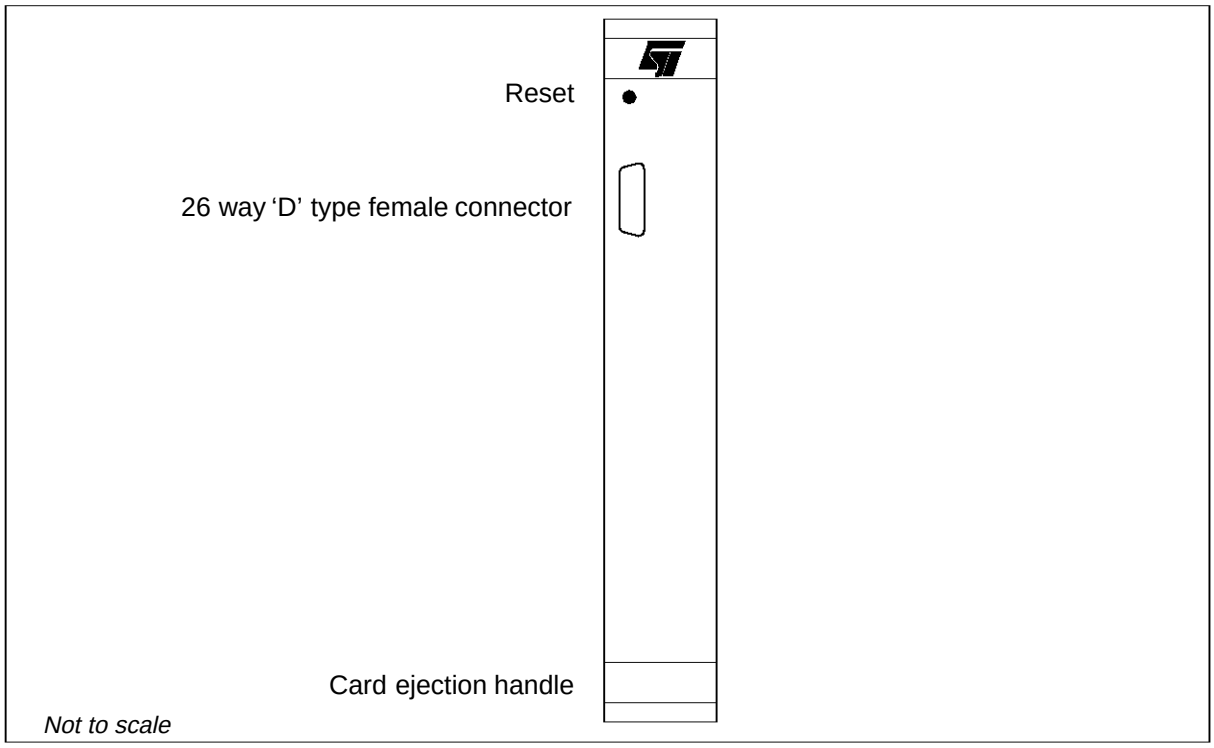

Figure 11.1 Front panel connections

Pin	Description	Pin	Description
1	**+notSSDownReset**	14	**GND**
2	**+notSSDownAnalyse**	15	**GND**
3	**+notSSDownError**	16	**GND**
4	**+notSSUpReset**	17	**GND**
5	**+notSSUpAnalyse**	18	**GND**
6	**+notSSUpError**	19	**-notSSDownReset**
7	**+LinkOut**	20	**-notSSDownAnalyse**
8	**+LinkIn**	21	**-notSSDownError**
9	**GND**	22	**-notSSUpReset**
10	**GND**	23	**-notSSUpAnalyse**
11	**GND**	24	**-notSSUpError**
12	**GND**	25	**-LinkOut**
13	**GND**	26	**-LinkIn**

Table 11.3 26 way 'D' type female connector pinout

12 Mezzanine I/O connector

12.1 Mezzanine design guide

The mezzanine I/O connector is provided to allow the prototyping of peripheral interfaces for the ST20450.

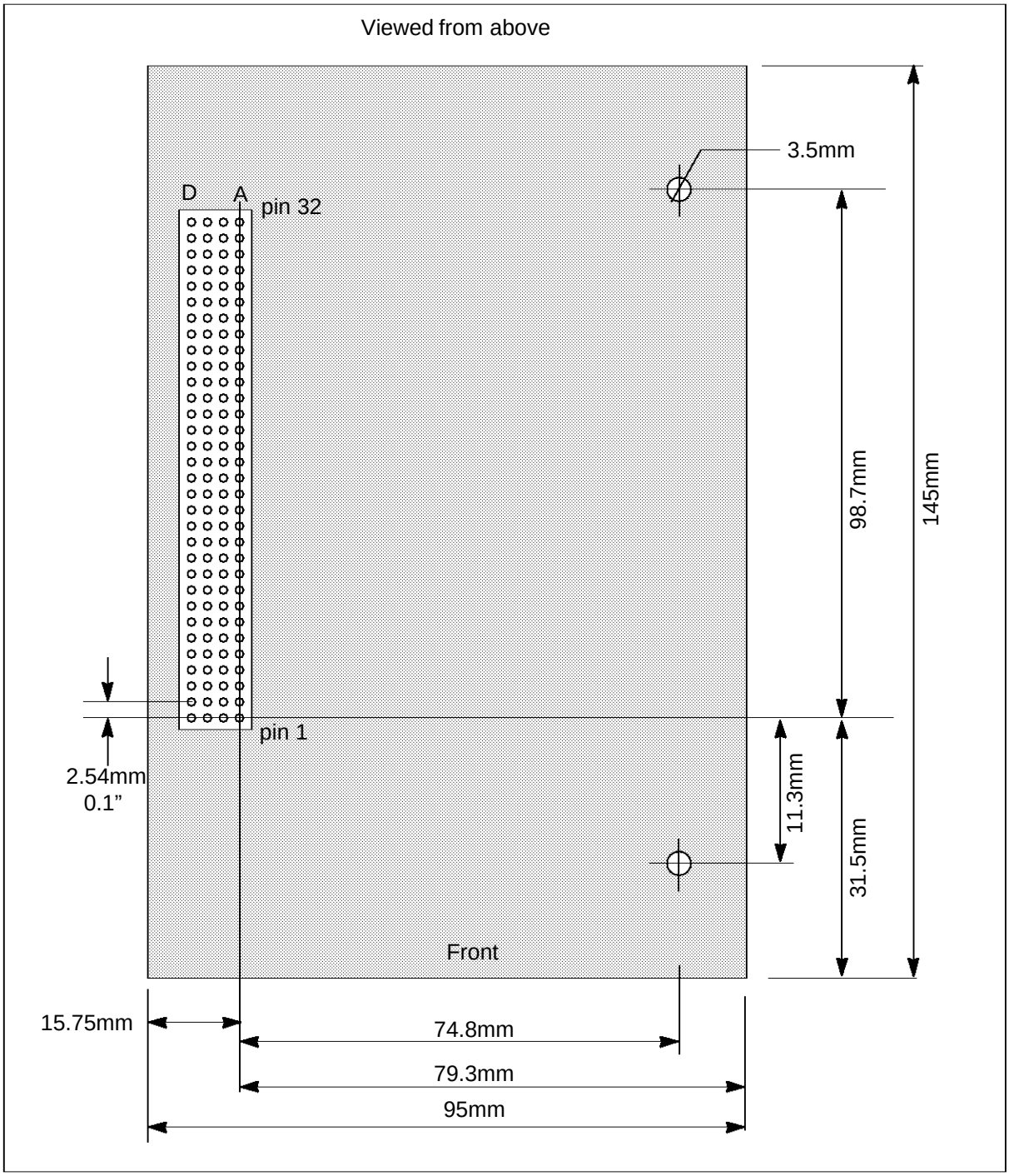

Figure 12.1 P4 and mezzanine board dimensions

Pin	Row D	Row C	Row B	Row A
1	**TAP(notTRST)**	**+5V**	**TAP(TDI)**	**TAP(TDO)**
2	**GND**	**TAP(TCK)**	**TAP(TMS)**	**+5V**
3	**notDMABE0**	**notDMABE1**	**notDMABE2**	**notDMABE3**
4	**notDMARAS**	**GND**	**notDMACAS**	**notDMAWr**
5	**3V3**	**Interrupt0**	**Interrupt1**	**GND**
6	**EventReq**	**EventAck**	**GND**	**Reset**
7	**MemReq**	**GND**	**MemGrant**	**MemRfPending**
8	**GND**	**notMemRf**	**MemWait**	**GND**
9	**notMemBE2**	**notMemBE3**	**GND**	**notMemRd**
10	**notMemPS2**	**GND**	**notMemBE0**	**notMemBE1**
11	**3V3**	**notMemRAS2**	**notMemCAS2**	**GND**
12	**A21**	**A22**	**GND**	**A23**
13	**A18**	**GND**	**A19**	**A20**
14	**GND**	**A16**	**A17**	**GND**
15	**A13**	**A14**	**GND**	**A15**
16	**A10**	**GND**	**A11**	**A12**
17	**3V3**	**A8**	**A9**	**GND**
18	**A5**	**A6**	**GND**	**A7**
19	**A2**	**GND**	**A3**	**A4**
20	**GND**	**D30**	**D31**	**GND**
21	**D27**	**D28**	**GND**	**D29**
22	**D24**	**GND**	**D25**	**D26**
23	**3V3**	**D22**	**D23**	**GND**
24	**D19**	**D20**	**GND**	**D21**
25	**D16**	**GND**	**D17**	**D18**
26	**GND**	**D14**	**D15**	**GND**
27	**D11**	**D12**	**GND**	**D13**
28	**D8**	**GND**	**D9**	**D10**
29	**3V3**	**D6**	**D7**	**GND**
30	**D3**	**D4**	**GND**	**D5**
31	**D0**	**GND**	**D2**	**D2**
32	**5V**	**ProcClock**	**+5V**	**+12V**

Table 12.1 I/O bus pinout - Hirose pinout

Input 3.3V	3.3V Input (5V tolerant)	3.3V only Output	3.3V Output (5V tolerant)	3.3V only bidirectional	5V output
notDMABE(3:0)	EventReq	notMemBE(3:0)	TAP(notTRST)	D(31:0)	Reset
notDMARAS	Interrupt(1:0)	notMemRAS2	TAP(TCK)	A(23:2)	
notDMACAS	TAP(TDO)	notMemCAS2	TAP(TDI)		
notDMAWr		notMemPS2	TAP(TMS)		
MemReq		notMemRd			
MemWait		EventAck			
		notMemRf			
		ProcClock			
		MemGrant			
		ProcClock			
		MemRfPending			

Note:
Outputs are defined as a signal coming from the ST20450 Development Board to the mezzanine card.

Table 12.2 Mezzanine connector pin classification

Care must be taken to use the correct voltage level for **VOut** pins on the ST20450. The databus is 3.3V only and a voltage level connection buffer must be used if interfacing to 5V peripherals. An example circuit is shown in Figure 12.2.

If DMA is used, a bidirectional buffer should be used for the address lines as well as for data.

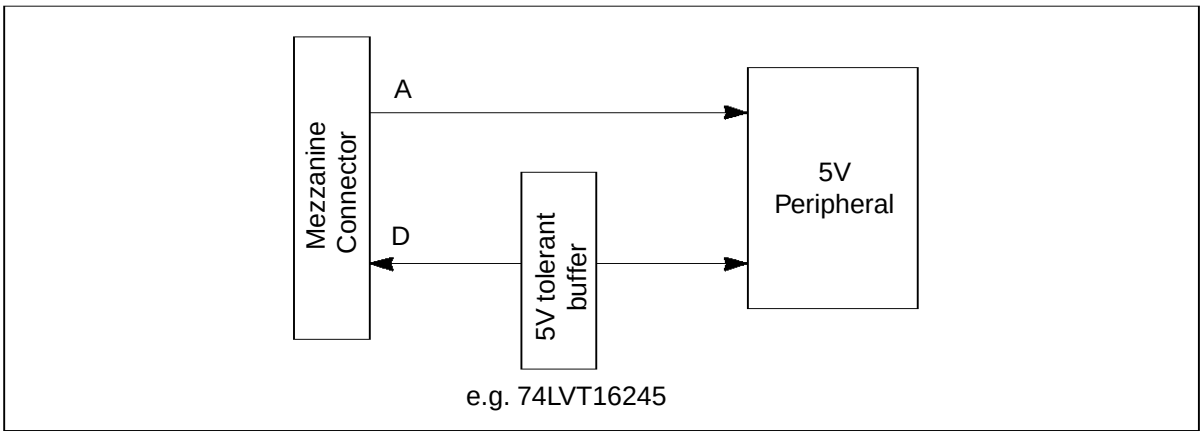

Figure 12.2 Interfacing to 5V peripherals

Since the address and databus are also connected to other devices on the ST20450 Development Board, only one TTL load is permitted on any signal.

For timing data, refer to the ST20450 datasheet.

12.2 DMA

The mezzanine interface can access the DRAM SIMMs using DMA. To access this, the following sequence must be followed.

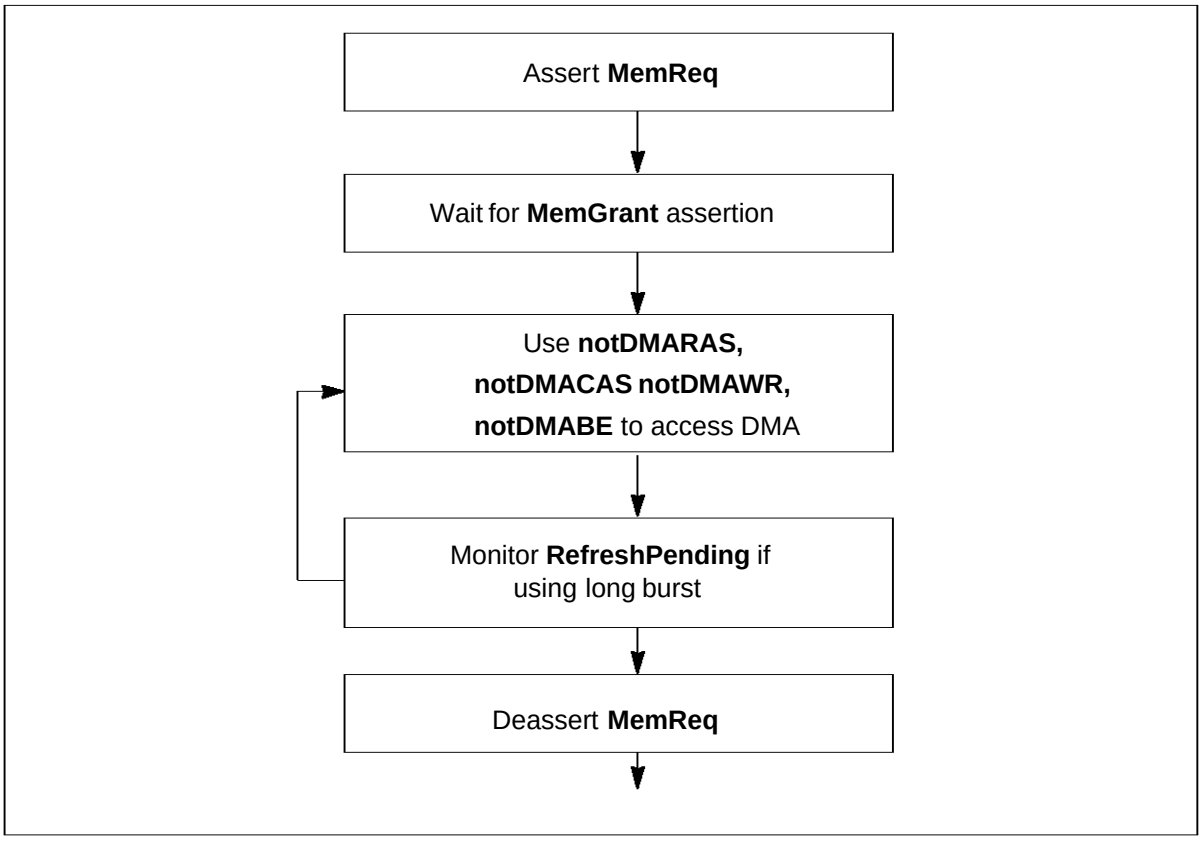

Figure 12.3 Access to DRAM SIMMs using DMA

The DMA signals are active low and when not in use should be held high, (3.3V).

notDMARAS, **notDMACAS** and **notDMAWR** signals enter the DRAM via a multiplexer. The **notDMA(3:0)** are used as byte enables to allow byte writes to the DRAM and the four **notCAS** strobes of the SIMM are generated as an OR of **notDMACAS** and **notDMABE(3:0).** Refer to Figure 12.4.

Note:

DMA access is only possible on boards of version ST20450-1C or later.

.

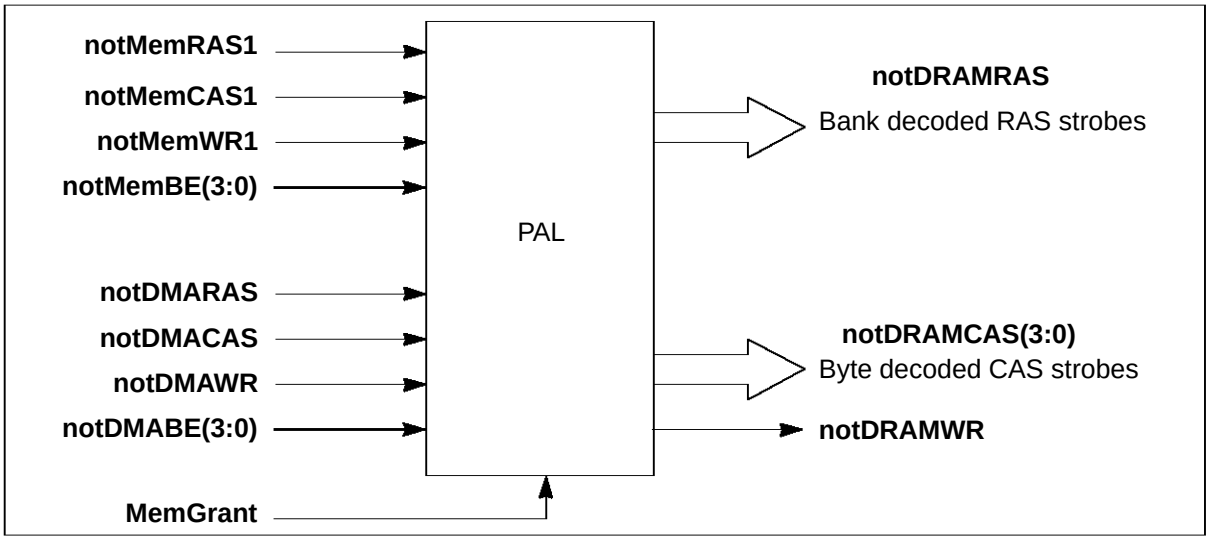

Figure 12.4

13 Clock source

The ST20450 has two separate clock inputs for the CPU clock and link clock. To enable the ST20450 to be driven at any frequency while still maintaining standard 10 or 20Mbit link speeds, the ST20450 Development Board has two crystal oscillator sockets - one in both IC45 and IC55. By default, the board is supplied with a 5MHz crystal in IC45 which connects to the ST20450 **LinkClockIn** and the interrupt generator clock. Jumper J5 is used to connect this crystal to the CPU **ClockIn** so that a single crystal oscillator is used to supply all the clocks required.

If an alternative CPU clock frequency is required, jumper J5 should be removed and a suitable crystal inserted into the IC55 socket. Jumpers J1(7:9) should be adjusted accordingly.

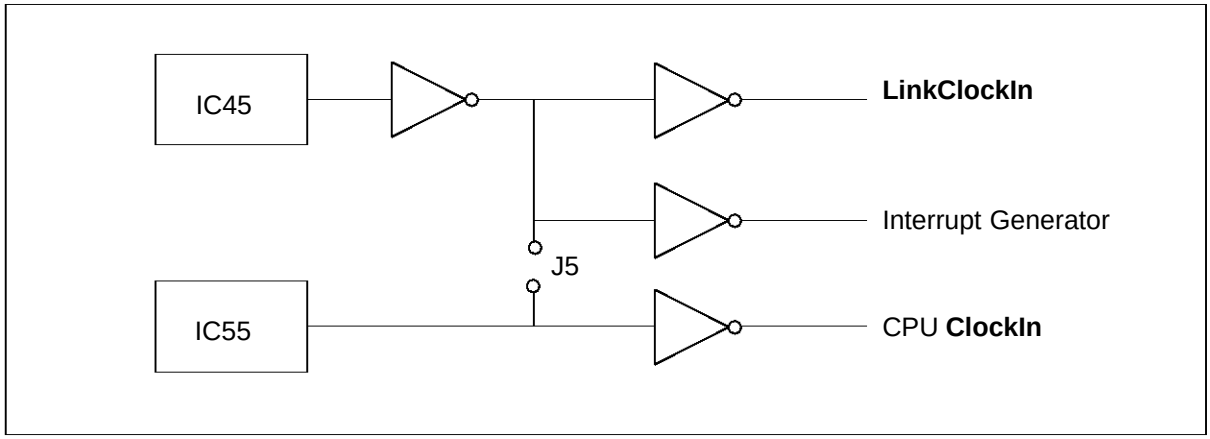

Figure 13.1 Clock source

14 Logic analyser connections

The board uses six 20 pin IDC header connectors to attach a logic analyser to the ST20450. The signals visible to the logic analyser are shown in Table 14.1.

Pin	POD1 ADDRESS (15:0)	POD2 ADDRESS (31:16)	POD3 DATA (15:0)	POD4 DATA (31:16)	POD5 STROBES	POD6 MISC
3(Clk)	notMemCAS0	notMemCAS1	notMemCAS2	notMemCAS3	User defined	ProcClock
4	MEMADD15	MEMADD31	MEMDATA15	MEMDATA31	EventWaiting	Debug7
5	MEMADD14	MEMADD30	MEMDATA14	MEMDATA30	MemRfPending	Debug6
6	MEMADD13	MEMADD29	MEMDATA13	MEMDATA29	MemGranted	Debug5
7	MEMADD12	MEMADD28	MEMDATA12	MEMDATA28	MemReq	Debug4
8	MEMADD11	MEMADD27	MEMDATA11	MEMDATA27	notMemRf	Debug3
9	MEMADD10	MEMADD26	MEMDATA10	MEMDATA26	notMemRd	Debug2
10	MEMADD9	MEMADD25	MEMDATA9	MEMDATA25	notMEMWRB1	Debug1
11	MEMADD8	MEMADD24	MEMDATA8	MEMDATA24	notMEMWRB0	Debug0
12	MEMADD7	MEMADD23	MEMDATA7	MEMDATA23	notMEMPS3	User defined
13	MEMADD6	MEMADD22	MEMDATA6	MEMDATA22	notMEMPS2	User defined
14	MEMADD5	MEMADD21	MEMDATA5	MEMDATA21	notMEMPS1	User defined
15	MEMADD4	MEMADD20	MEMDATA4	MEMDATA20	notMEMPS0	User defined
16	MEMADD3	MEMADD19	MEMDATA3	MEMDATA19	notMEMRAS3	User defined
17	MEMADD2	MEMADD18	MEMDATA2	MEMDATA18	notMEMRAS2	MemWait
18	notMEMWRB3	MEMADD17	MEMDATA1	MEMDATA17	notMEMRAS1	ResetResponse
19	notMEMWRB2	MEMADD16	MEMDATA0	MEMDATA16	notMEMRAS0	Reset
20	GND	GND	GND	GND	GND	GND

Table 14.1 Logic analyser POD assigned pinouts

15 Interrupt counter

The ST20450 Development Board has interrupts 0 and 1 connected directly to the mezzanine connector and interrupt 2 is connected to a 10 bit countdown timer. Using this countdown timer it is possible for software to set an interrupt in the future to test interrupt software response.

The timer has two associated registers to control it, **CountDisable** and **CounterStart** value. To operate the timer the following sequence needs to be run:

1 Set up the interrupt registers within the ST20450 to enable interrupt 2.

2 Write a 1 into the counter disable register to stop the timer. This will also set the interrupt line to 0.

3 Write the starting value for the counter into the counter start value register.

4 Write a 0 into the counter disable register. This now enables the counter and it will count down to zero using a 5MHz input clock. Once the counter reaches zero it sets the interrupt. On the next clock cycle, the interrupt will be cleared and the counter reset to the counter start value and continues to count down to zero.

16 Operating Ranges

Functionality is not guaranteed outside the Operating Ranges. Operation beyond the Operating Ranges is not recommended and may affect device reliability.

Parameter	Min.	Typ.	Max.	Unit	Note
Operating temperature	0		50	^{o}C	
Airflow	0			m/s	
+5V DC	4.875	5	5.25	V	
Power consumption, not including mezzanine board			7	W	
Power available to mezzanine (+12V dc Max)			10	W	
Power available to mezzanine (+5V dc Max)			20	W	1
Power available to mezzanine (+3.3V dc Max)			15	W	1
Any temperature sensitive parts should be designed such that the board can be placed on a desk with no airflow and still be within the silicon's working temperature range.					

Table 16.1 Operating Ranges

1 Total 3.3V plus 5V power consumption should not exceed 30W.

16.1 Absolute maximum ratings

Functionality at or above these limits is not implied. Stresses beyond the Absolute Maximum Ratings may cause permanent damage.

Parameter	Min.	Max.	Unit
Storage temperature	0	70	^{o}C
Supply Voltage	0	7.0	V

Table 16.2 Absolute Maximum Ratings

17 Field Support

SGS-THOMSON Microelectronics Limited products are supported worldwide through Sales Offices and authorized distributors.

18 Ordering information

Description	Order Number
ST20450 Development Board VME format multi-role development board	ST20450-SAB

Table 18.1 Ordering information

19 References

1 *ST20450 32 bit microprocessor datasheet*, SGS-THOMSON Microelectronics Limited, 1995, 42 1626 xx.

Appendix A

A.1 IMEM file example

```
-- -----
--
--      Memory configuration file produced
--      for the ST20450 Development Board.
--      on 16th May, 1995
--
-- -----

Processor.Type        := T450
Dram.Refresh.Interval := 320 Cycles
Dram.Refresh.Time     := 4 Cycles
Dram.Refresh.RAS.High := 3 Phases
Signal.All.Pending.Cycles
Proc.Clock.Out       := enabled

Pad.Strength.Rcp0    := 2
Pad.Strength.Rcp1    := 2
Pad.Strength.Rcp2    := 2
Pad.Strength.Rcp3    := 2
Pad.Strength.Be1     := 2
Pad.Strength.Be2     := 2
Pad.Strength.A2.8    := 2
Pad.Strength.A9.12   := 2
Pad.Strength.A13.16  := 2
Pad.Strength.A17.20  := 2
Pad.Strength.A21.24  := 2
Pad.Strength.A25.31  := 2
Pad.Strength.D0.7    := 2
Pad.Strength.D8.15   := 2
Pad.Strength.D16.31  := 2


Bank 0 ”Bank0 - 512K of SRAM”
    Device.Type             := Non-Dram
    Wait.Pin                := disabled
    Port.Size               := 32 bits

    Ras.Strobe ”S1”
        Inactive
    End.Strobe

    Cas.Strobe ”notCS”
        Falling.Edge.Active.During       := Read & Write
        Rising.Edge.Active.During        := Read & Write
        Time.To.Falling.Edge             := 0 Phases
        Time.To.Rising.Edge              := 4 Phases
    End.Strobe
```

```
    Programmable.Strobe ″notOE″
        Falling.Edge.Active.During       := Read
        Rising.Edge.Active.During        := Read
        Time.To.Falling.Edge             := 0 Phases
        Time.To.Rising.Edge              := 4 Phases
    End.Strobe

    Write.Strobe ″notMemWrB″
        Falling.Edge.Active.During       := Write
        Rising.Edge.Active.During        := Write
        Time.To.Falling.Edge             := 1 Phases
        Time.To.Rising.Edge              := 3 Phases
    End.Strobe

    Cas.Cycle.Time          := 2 Cycles
    Bus.Release.Time        := 1 Cycles
    Data.Drive.Delay        := 0 Phases

End.Bank


Bank 1 ″DRAM BANK 1″
    Device.Type             := Dram
    Wait.Pin                := disabled
    Port.Size               := 32 bits
    Page.Address.Bits       := 003FF000
    Page.Address.Shift      := 10 bits

    Ras.Strobe ″notRAS″
        Falling.Edge.Active.During       := Read & Write
        Time.To.Falling.Edge             := 0 Phases
    End.Strobe

    Cas.Strobe ″notCAS″
        Falling.Edge.Active.During       := Read & Write
        Rising.Edge.Active.During        := Read & Write
        Time.To.Falling.Edge             := 2 Phases
        Time.To.Rising.Edge              := 12 Phases
    End.Strobe

    Programmable.Strobe ″notWrite″
        Falling.Edge.Active.During       := Write
        Rising.Edge.Active.During        := Write
        Time.To.Falling.Edge             := 0 Phases
        Time.To.Rising.Edge              := 12 Phases
    End.Strobe

    Write.Strobe ″notBE″
        Falling.Edge.Active.During       := Read & Write
        Rising.Edge.Active.During        := Read & Write
        Time.To.Falling.Edge             := 0 Phases
        Time.To.Rising.Edge              := 12 Phases
    End.Strobe
```

```
    Ras.Precharge.Time      := 4 Cycles
    Ras.Edge.Time           := 2 Phases
    Ras.Edge.Active.During  := Read & Write
    Ras.Cycle.Time          := 2 Cycles
    Cas.Cycle.Time          := 6 Cycles
    Bus.Release.Time        := 1 Cycles
    Data.Drive.Delay        := 0 Phases

End.Bank
```